**Proposal Master Thesis at INTEL**

**VIRTUAL PROTOTYPING**  
**DIGITAL DESIGN & VERIFICATION**  
**SYSTEM ARCHITECTURE**  
**RF PHYSICAL DESIGN – LAYOUT**  
**SENIOR FIRMWARE ENGINEERING**  
**ANALOG CIRCUIT DESIGN**  
**LOW POWER OPTIMIZATION**  
**PROJECT MANAGEMENT**  
**DESIGN FLOW & TOOL DEVELOPMENT**

**Topic:**  
**High-Level Synthesis (HLS) Assisted Implementation of Complex DSP Chains**

**Description:**

The methodology of High-Level Synthesis (HLS) allows the semi-automatic generation of hardware descriptions on RTL from models specified in a high-level language (SystemC).

In this thesis, HLS should be used for the implementation of complex DSP chains (e.g. LTE baseband signal generation). The goal is to provide various functional HLS-generated implementations using different micro-architectures. Finally, the quality of results (QoR) of HLS-generated hardware should be compared with the results of different implementation methodologies (e.g. Simplify DSP block set, handcrafted RTL code).

**Summary of Tasks:**

- Modeling the DSP chain in SystemC  
- Read up on the basics of HLS  
- Become acquainted with a commercial HLS tool  
- Adoption of SystemC models for using them with the HLS tool  
- Explore different implementations on RTL using the HLS tool  
- Compare QoR of HLS-generated hardware and hardware from other implementation methodologies

**Required skills:**

- Strong interest in digital hardware design (VHDL, digital design flow, ...)  
- Knowledge in C/C++ programming  
- Knowledge in SystemC programming desirable but not required

**Qualification:**

- Master student of computer sciences, information electronics, Mechatronics or similar (JKU / FH / TU)
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Topic:

Efficiency improvement of Rapid Prototyping verification suite by importing/exporting RTL test cases

Description:

Rapid Prototyping is used in Digital Design Verification to improve the verification coverage. The number of executed test cases can be increased due to shorter execution time for one test case. The additional usage of a processor on the Rapid Prototyping System allows increasing the number of test cases by using test case templates with variables which are updated loop based or random based.

The Rapid Prototyping verification is slowed down by creating the test cases and by analyzing the test case fails. An improvement with a closer connection between RTL and FPGA test cases should be analyzed.

The goal of this work is to go beyond this and to bring the user with an approach to effectively:
- Reuse an existing FPGA regression suite and adapt it to the new ARM Versatile board.
- Reuse RTL verification environment for an existing design under test.
- Create an importing tool for RTL test cases / create an exporting tool for FPGA test cases.
- Perform the FPGA verification flow with the standard approach (-es) including creating test case/fail analysis.
- Perform the improved FPGA verification flow including creating test case/fail analysis.
- Compare the approaches in a realistic situation.

Related to this work, but not required, the following points could be considered:
- Using the previous work of RTL test case generation tool

This internship is a great opportunity to acquire a strong experience in:
- Digital Design development
- Rapid prototyping
- Software development
- Linux on ARM and Questa tools

Qualification:
- Master thesis for students ESD "Embedded System Design" @ FH Hagenberg
- Master thesis for students of computer sciences, information electronics @ JKU
Proposal Bachelor Thesis at INTEL

Topic:

**Eclipse CDT IDE customization for embedded software development**

Description:

Eclipse CDT is a standard integrated development environment (IDE) for C/C++ development. The CDT plugin is customizable and expandable. However, for embedded software development there are specific requirements which cannot be covered by built-in customization options.

**The goal** of this thesis is a fully integrated IDE based on Eclipse CDT fulfilling all special requirements stemming from embedded C development. The student will receive a requirement list and has to provide a solution by either integrating suitable off-the-shelf plugins or developing a custom plugin in Java.

Main challenges:

- Familiarization with firmware development specifics
- Research to identify suitable off-the-shelf plugins
- Usability evaluation of identified plugins
- Requirements definition for custom plugin development
- Design and concept for custom plugin development
- Implementation and testing

Required skills:

- Strong interest in software engineering
- Knowledge in Java programming
- Knowledge in Eclipse plugin development preferred
- Knowledge in embedded software development is not required

Qualification:

- Bachelor student in computer sciences or similar
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Topic:

SystemC on Nvidia GPUs

Description:

Virtual Prototyping is a state of the art methodology to enable efficient firmware development and verification. Since systems are getting more and more complex, simulation speed is critical to enable proper development turnaround times. Especially when the level of required details is very high (e.g. low-level firmware development). Currently all simulations are executed on one processor without making use of parallel computing approaches.

The target objective of this thesis is to speed up the simulation performance of SystemC designs at different level of abstraction by exploiting the high degree of parallelism afforded by today’s general purpose graphics processors.

Main challenges:

- Familiarization with parallel computing approaches
- Familiarization with SystemC kernel details
- Familiarization with different SystemC designs
- Analysis and design partitioning/restructuring
- Implementation of an example and testing

Required skills:

- Strong interest in parallel computing
- Strong interest in SystemC modeling and simulation cycle
- Knowledge in software development

Qualification:

- Master student in computer sciences or similar
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Topic:

Automatic generation of an abstract Virtual Prototype based on UML descriptions for RF transceiver applications

Description:

Virtual Prototyping is a state of the art methodology for verification and validation of complex systems. The different use-models for Virtual Prototypes require different flavors of models. In this thesis we want to develop a purely state-based transceiver model which is demanded for high-level software development and system simulation.

The goal of this thesis is to enable SystemC code generation of a high-level model based on state-chart descriptions in UML (Unified Modeling Language). This model has to be verified in our existing development framework.

Main challenges:
- Familiarization with radio transceiver specifics
- Familiarization with code generation approaches
- Analysis of currently existing VP solutions and design definitions (UML - Unified Modeling Language)
- Participation in a concept development for an abstract VP
- Implementation of templates, model generation and verification

Required skills:
- Strong interest in modeling of hardware components for Virtual Prototype applications
- Knowledge in SystemC programming
- Knowledge in software development in general

Qualification:
- Bachelor student in computer sciences or similar
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Topic:

A SystemC transaction-level-model (TLM) for a time-triggered-architecture (TTA) processor

Description:

A time-triggered-architecture (TTA) processor is an ideal processor template for application specific instruction set processors (ASIP) with customized data path, but without the inflexibility and design cost of fixed function hardware accelerators. For the Virtual Prototype a SystemC model of this processor is required. Transaction-level-modeling is the state of the art modeling approach. The current existing model is clock-based and needs to be adapted.

The goal of this thesis: to analyze the existing framework for SystemC and to refactor the existing model. Concept definition, implementation and verification of a transaction-level based model are as well parts of this thesis.

Main challenges:
- Familiarization with time-triggered-architecture (TTA) processor
- Evaluation and refactoring of the existing clock-based model and flow
- Requirements definition for the model
- Concept, implementation and verification
- Performance and timing accuracy analysis

Required skills:
- Strong interest in transaction-level modeling
- Strong interest in processor architectures
- Knowledge in SystemC modeling
- Knowledge in transceiver concepts is not required

Qualification:
- Bachelor student in computer sciences or similar
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Topic:

Real time challenges for next generation radio transceiver firmware

Description:

The firmware inside next generation radio transceivers has “hard” real-time constraints for implementing the sequencing of 2G/3G/4G radio accesses. Many systems use an Operating System-less, interrupt driven firmware approach, which makes priority based task scheduling a challenging task.

The goal of this thesis is an evaluation of the applicability of existing open source embedded real-time OS (RTOS) implementations to RF Transceiver control architectures featuring scalable CPU cores, i.e.:

- Features, requirements and trade-offs in implementing different levels of concurrency (e.g. tasks/threads/interrupts, et.al.).
- Cost in terms of hardware (supporting CPU features) and software (runtime overhead and OS memory footprint) and the limiting factors w.r.t. RF transceiver real-time runtime requirements.
- Porting of an RTOS implementation to the existing infrastructure.
- Estimation of use cases which amortize the resource overhead of an RTOS.
- Selection and execution of a representative set of benchmarks.

Qualification:

- Master thesis for students ESD ”Embedded System Design” / Software Engineering @ FH Hagenberg
- Master thesis for students of computer sciences, information electronics, Mechatronics or similar @ JKU

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Topic:

**Object oriented languages for resource limited embedded systems**

Description:

The firmware inside next generation radio transceivers has “hard” real-time constraints for implementing the sequencing of 2G/3G/4G radio accesses. Such constraints mostly yield in the selection of plain C as language of choice in embedded systems programming. Many features of thus ignored object oriented languages and design principles would however be nice to find in such projects from a software engineering point-of-view.

The goal of the thesis is to evaluate the applicability of object oriented extensions in the implementation of next generation radio transceiver firmware:

- Reference Implementation of some representative parts of RF transceiver firmware using the existing infrastructure.
- Benchmarking performance / code-size / modularity / code re-use against existing C implementations.
- Conclusion on which parts of RF transceiver firmware could benefit for object oriented design at reasonable low performance / resource usage overhead.

Qualification:

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Topic:

Tools for Analysis and Debugging of distributed messaging systems in NG radio transceivers

Description:

Computational needs for implementing tomorrow’s radio access technologies in radio transceivers keep increasing. Driving system performance through clock frequency scaling soon leads to a dead end, which especially holds for embedded systems where power consumption and its dissipation matter more than anything. Thus implementing scaling through parallelization using multiple message coupled cores is reasonable. Such distribution systems however are harder to debug and one way to do so is by capturing traces of inter-core communication and graphically analyze those traces for erroneous behavior.

The goal of this thesis is an evaluation of the applicability of existing message based debugging tools and their applicability to a multicore and message coupled RF Transceiver control architecture implementation:

- Evaluation of available file formats for storing communication traces and graphical debuggers for analyzing traces from a real world distributed embedded system.
- Implementation of a tool for converting the existing RF transceiver hardware tracing output into a format suitable for use with the most appropriate message based debugger selected.
- Evaluation of the selected debugging tool.

Qualification:

- Master thesis for students ESD "Embedded System Design" @ FH Hagenberg
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**Topic:**  
Automatisierte Entwurfsmethode für digitale Signalverarbeitungsschaltkreise mit leistungseffizienter Struktur

**Beschreibung:**
Moderne digitale Signalverarbeitungsschaltkreise für die digitale Signalverarbeitung werden immer wichtiger. Die Anzahl solcher Blöcke nimmt immer mehr zu.

**Ziel der Arbeit ist:**

![Diagram of a filter structure](image)

**Aufgaben und Voraussetzungen:**
- Implementierung eines Tools zur Generierung von digitalen Filterstrukturen in RTL (ASAP, ASFIR, ...)
- Verifikation der richtigen Funktionalität des generierten VHDL Filterdesigns (Vergleich mit Matlab Modell)
- Test-Synthese des generierten VHDL Filterdesigns (Synopsys Design Compiler)
- C/C++, Python/Perl Skript Programmierung, Questasim
- Digital Hardware Design (VHDL, Digital Design Flow, ...)

**Qualifikation:**
- Master thesis for students ESD "Embedded System Design" @ FH Hagenberg
- Master thesis for students of Informatik/Informationselektronik/Mechatronik @ JKU

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Topic: **Optimal Digital Loop Filter in the Presence of Excess Loop Delay**

Description:

The noise transfer function of RF Digital Phase locked loops (DPLL) used in state of the art communication devices is one part which defines the purity of the generated RF output signal. Digital signal processing in digital PLLs adds latency to the loop which reduces the achievable phase margin and leads to phase peaking of the closed loop transfer function.

Actually used loop filter types do not take this delay into account. The application of modern control theory like predictive control based on state observation respectively state prediction could help to find an optimized loop filter which enables higher performance needed for future high data rate communication standards.

Goals:

- Derive an alternative loop filter topology which takes into account latency of the loop
- Compare the noise transfer function of the new filter with the existing solution
- (optional) Give a proposal for loop filter implementation

Qualification:

- Control Engineering
- Digital Signal Processing
- Matlab
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Topic:

Simulation of a Stochastic Flash TDC for Divider Based PLLs

Description:

Continuous increase of data rates in modern mobile communication standards set demands of improved purity of the generated RF signals. A limiting factor for the achievable purity is the in-band noise of the Phase Locked Loop (PLL).

As the use of digital PLLs is preferred in advanced CMOS technologies, the Time-to-Digital Converter (TDC) quantization noise is the main contributor to the in-band noise. An approach to realize very fine quantization is the Stochastic Flash TDC, which makes use of statistical properties of parallel switching elements in order to detect and quantize a time delay. Proposals for such circuits exist, but they have to be analyzed in the application of divider based PLLs.

Goals:

- Generate a Matlab time domain model of a Stochastic Flash TDC which can be used in a divider based DPLL
- Simulate the TDC model in the context of an existing time domain DPLL model
- Identify limitations considering circuit imperfections and evaluate possibilities to improve design, calibration, etc.

Qualification:

- Good knowledge of Matlab, Digital Signal Processing, Mixed Signal Circuit Design
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SENIOR Firmware ENGINEERING
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PROJECT MANAGEMENT
DESIGN FLOW & TOOL DEVELOPMENT

Topic:
Effects of Multi-Rate Modulation in a
digital PLL Two-Point Modulator

Description:
RF Phase modulators in state of the art communication devices use a Digital PLL with two-point modulation scheme to provide high modulation bandwidth. Both paths have to match accurately in order to guarantee distortion-free modulation. However, due to the different sample rates of the two insertion points, exact matching is not possible. Actual implementations show that the reached performance is sufficient, but future communication standards demand even higher bandwidths which make matching accuracy increasingly important.

Goals:
- Generate a discrete time model of the combined modulation paths
- Show the modulation transfer function and prove with time domain simulation
- Check influences on actual modulation standards
- Estimate bandwidth limitations of an existing phase modulator
- (optional) Propose modifications to overcome limitations

Qualification:
- Matlab, Communications Engineering, Control Engineering, Digital Signal Processing
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RF PHYSICAL DESIGN – LAYOUT
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Topic:

Enhanced Sample Rate Conversion in a Digital PLL Two-Point Modulator

Description:

In order to align the modulation data to the non-equidistant digital sampling on the RF side and to shift repetition spectra to higher carrier offset frequency’s a sample rate conversion is done inside the phase and amplitude modulation paths of the polar modulator. The sample rate conversion between an equidistant and non-equidistant clock domain is done by a variable interpolation based on the knowledge of the frequency modulation and DPLL locking frequency.

However, the interpolation and trajectory movements are calculated on the equidistant digital side and interpolation errors result due to certain assumptions and simplifications resulting in additional in-band and out-of-band errors characterized by EVM and spectral emission.

Goals:

- Analyze the current interpolation mechanism and derive an mathematical model
- Propose ways to improve the interpolation and reduce interpolation errors
- Show the functionality by Matlab simulations in the context of an existing time domain DPLL model
- (optional) Propose hardware modifications to adapt to the new interpolation structure

Qualification:

- Matlab, Communications Engineering, Control Engineering, Digital Signal Processing

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### Topic:

**An Analytical Description of the Relation between Phase Error, EVM and DPLL Loop Bandwidth with respect to Asymmetric and Clustered RB Allocation Scenarios in LTE Uplink Transmission**

### Description:

From system simulations it is observed, that the trade-off between different noise sources determining the DPLL loop bandwidth and contributed phase error due to noise has different impacts on EVM depending on the resource block (RB) allocation in LTE Uplink. In order to optimize the DPLL configuration based on the current RB allocation a deeper understanding of the relation between spectral characteristics of the phase/frequency modulation signal and the complex IQ signal after recombination of amplitude and phase is necessary.

### Goals:

- Check if a qualitative and quantitative relation between the polar and complex IQ signals can be derived with respect to certain RB allocation scenarios in LTE Uplink
- Analyze the RB allocation dependent effect of phase noise / loop bandwidth on Phase Error and EVM
- Verify and show your results by simulations in Matlab

### Qualification:

- Matlab, Signal and System Theory, Digital Signal Processing
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Topic:
Application of redundant binary representations in the design of low-power DSP hardware algorithms

Description:
Reducing the power consumption in digital frontends within RF transceiver devices is an active field of research. Dedicated DSP hardware is custom-tailored to attain ambitiously low power consumption targets. A significant advantage of redundant binary representations (RBR) compared to a standard two's-complement (2CR) representation is the absence of carry propagations, which constitute a significant contribution to the overall switching activity of digital logic.

Summary of Tasks:
- Conduct a survey of RBRs suitable for implementing domain-specific algorithms.
- Convert selected blocks from an existing DSP chain from 2CR to RBR (VHDL/Verilog design) and ensure synthesizability using Synopsys DC.
- Evaluate the use of high-speed vector compression blocks for addition and multiplication of RBRs (4-2 compressors, fused-MACs, Synopsys DW02_tree).
- Implement HDL arithmetic operator library to facilitate design process.
- Quantify actual power consumption of converted DSP blocks with real-world activity patterns using Apache PowerArtist.
- Optional: evaluate fraction range compression using PN² recoding
  - Determine feasibility of applying truncation rounding directly on recoded RBRs instead of converting back to 2CR.
  - Determine optimum fraction range compression to minimize switching activity for zero values in RBR.

Qualification:
- Master student of computer sciences, information electronics, Mechatronics or similar (JKU / FH / TU)
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SYSTEM ARCHITECTURE
RF PHYSICAL DESIGN – LAYOUT
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Topic:

Automatic generation of temporal SystemVerilog properties based on UML interaction diagrams

Description:
One way to manage the steadily increasing hardware complexity of RF transceiver devices is the use of property-based verification. Attaining sufficient functional coverage in the pre-silicon verification phase is crucial to avoid costly silicon respins. Implementing (temporal) property checking of complex mixed-signal systems provides numerous benefits:

- Documents functionality as executable specification
- Improves observability by reporting errors close to their root cause
- Allows implementation of automatic quality gates for continuous delivery flows
- Formal- and simulation-based verification methodologies can use the same properties

Summary of Tasks:

- Participate in defining domain-specific UML sequence diagrams using SparxSystems Enterprise Architect.
- Extend an existing UML 2.1 XML parser (written in Python) by adding suitable data models for exported UML interaction diagrams (communication, sequence and timing diagrams).
- Use the newly defined data models to generate SystemVerilog temporal properties, preferably by implementing corresponding MAKO templates (http://www.makotemplates.org/)
- Optional: implement additional MAKO templates to generate register checking quality gates for post-silicon verification

Qualification:

- Bachelor student of computer sciences, information electronics, Mechatronics or similar (JKU / FH / TU)
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RF PHYSICAL DESIGN – LAYOUT
SENIOR Firmware ENGINEERING
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PROJECT MANAGEMENT
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Topic:
Accelerating RF transceiver firmware algorithms by flexible ASIP structures based on transport triggered architectures

Description:
Algorithms in the RF transceiver domain require highly specialized processing. Application-specific instruction-set processors (ASIP) deliver greater computational efficiencies than general purpose processors and more flexibility than fixed-function RTL designs. Combining firmware (FW) algorithms and programmable hardware (HW) accelerators increases algorithm performance while avoiding the design complexity of full HW implementations. Transport triggered architectures (TTA) are suitable ASIP structures with a wide range of applications in the RF transceiver domain (apart from power-critical DSP algorithms). Fast development turnaround cycles are achieved by using the open source TCE framework (http://tce.cs.tut.fi/), which includes a GUI for TTA design & simulation and a HDL code generator.

Summary of Tasks:
- Participate in identifying timing-critical FW algorithms, which can benefit from ASIP HW acceleration
- Evaluate different TTA structures including domain-specific function units (FU) regarding program size, resource usage, execution speed and silicon area
- Extend an existing FW tool-chain to provide direct control over newly defined TTAs
- Implement a flexible program code memory controller, including support for an existing DMA controller
- Optional: Evaluate TTAs as a replacement for full-custom high-speed interface protocol engines

Qualification:
- Master student of computer sciences, information electronics, Mechatronics or similar (JKU / FH / TU)